80286 microprocessor

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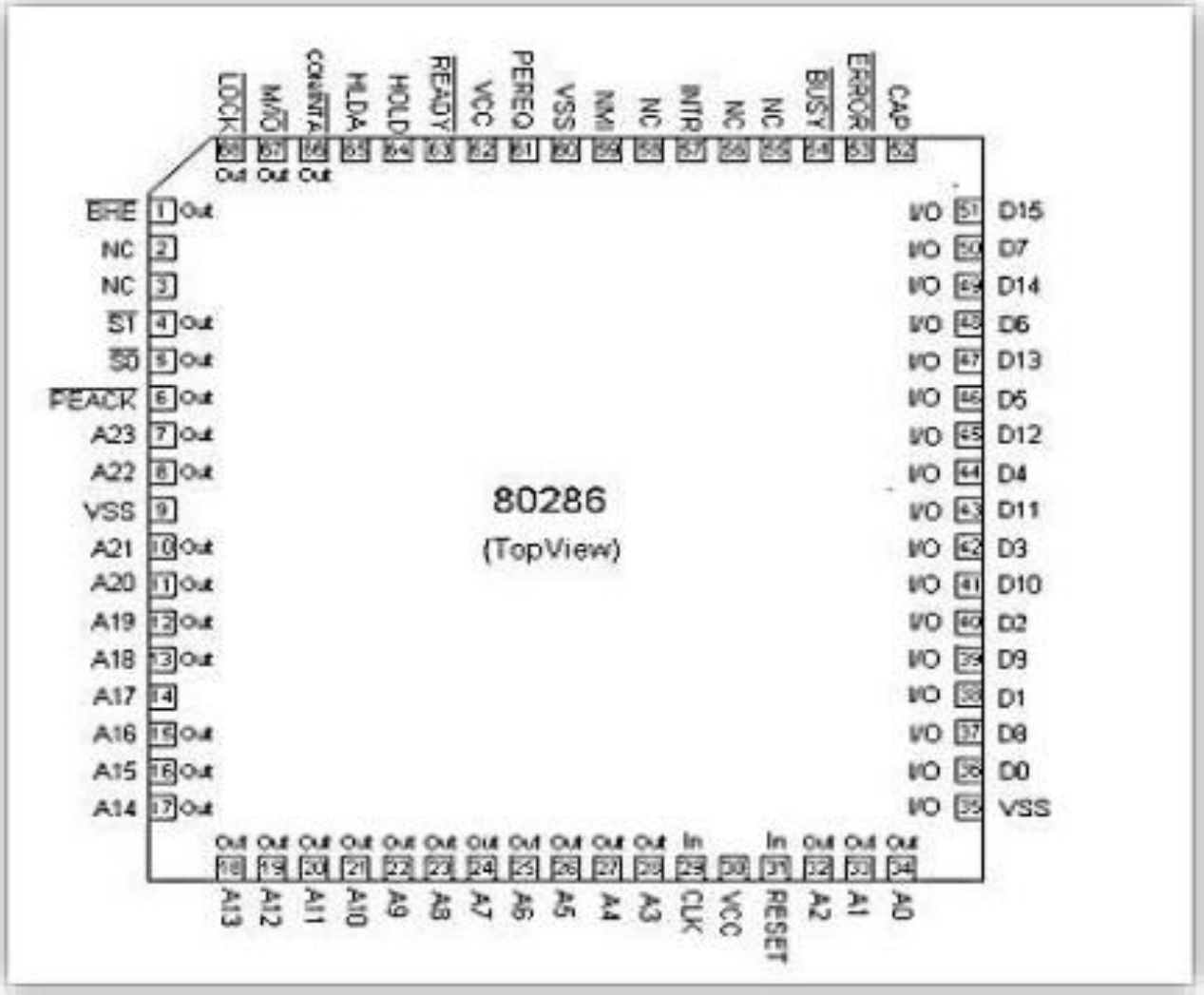
Introduction

- 80286 Microprocessor is a 16-bit microprocessor that has the ability to execute 16-bit instruction at a time. It has non-multiplexed data and address bus. The size of data bus is 16-bit whereas the size of address bus is 24-bit.
- It was invented in February **1982** by **Intel**. 80286 microprocessor was basically an advancement of 8086 microprocessor. Further in 1985, Intel produced upgraded version of 80286 which was a 32-bit microprocessor.
- It was the first 8086-based CPU with separate, non-multiplexed address and data buses and also the first with memory management and wide protection abilities. The 80286 used approximately 134,000 transistors in its original nMOS (HMOS) incarnation and, just like the contemporary 80186, it could correctly execute most software written for the earlier Intel 8086 and 8088 processors.
- Intel's first 80286 chips were specified for a maximum clockrate of 4, 6 or 8 MHz and later releases for 12.5 MHz.

Features

- It has non-multiplexed address and data bus that reduces operational speed.
- The addressable memory in case of 80286 is 16 MB.
- It offers an additional adder for address calculation.
- 80286 has faster multipliers that lead to quick operation.
- The performance per clock cycle of 80286 is almost twice when compared with 8086 or 8088.

80286 Pin Diagram



- **CLK:** This is the system clock input pin. The clock frequency applied at this pin is divided by two internally and is used for deriving fundamental timings for basic operations of the circuit. The clock is generated using 8284 clock generator.

- **D15-D0:** These are sixteen bidirectional data bus lines.
- **A23-A0:** These are the physical address output lines used to address memory or I/O devices. The address lines A23 - A16 are zero during I/O transfers

- **BHE:** This output signal, as in 8086, indicates that there is a transfer on the higher byte of the data bus (D15 – D8) .

- **S1** , **S0:** These are the active-low status output signals which indicate initiation of a bus cycle and with M/IO and COD/INTA, they define the type of the bus cycle.

- **M/ IO:** This output line differentiates memory operations from I/O operations. If this signal is it “0” indicates that an I/O cycle or INTA cycle is in process and if it is “1” it indicates
- that a memory or a HALT cycle is in progress.

- **COD/ INTA:** This output signal, in combination with M/ IO signal and S1 , S0 distinguishes different memory, I/O and INTA cycles.

- **LOCK:** This active-low output pin is used to prevent the other masters from gaining the control of the bus for the current and the following bus cycles. This pin is activated by a "LOCK" instruction prefix, or automatically by hardware during XCHG, interrupt acknowledge or descriptor table access
- **READY** This active-low input pin is used to insert wait states in a bus cycle, for interfacing low speed peripherals. This signal is neglected during HLDA cycle.

- **HOLD and HLDA** This pair of pins is used by external bus masters to request for the control of the system bus (HOLD) and to check whether the main processor has granted the control (HLDA) or not, in the same way as it was in 8086.

- **INTR:** Through this active high input, an external device requests 80286 to suspend the current instruction execution and serve the interrupt request. Its function is exactly similar to that of INTR pin of 8086.

- **NMI:** The Non-Maskable Interrupt request is an active-high, edge-triggered input that is equivalent to an INTR signal of type 2. No acknowledge cycles are needed to be carried out.

- **PEREG** and **PEACK** (**Processor Extension Request and Acknowledgement**)

- Processor extension refers to coprocessor (80287 in case of 80286 CPU). This pair of pins extends the memory management and protection capabilities of 80286 to the processor extension 80287. The PEREQ input requests the 80286 to perform a data operand transfer for a processor extension. The PEACK active-low output indicates to the processor extension that the requested operand is being transferred.

- **BUSY** and **ERROR:** Processor extension BUSY and ERROR active-low input signals indicate the operating conditions of a processor extension to 80286. The BUSY goes low, indicating 80286 to suspend the execution and wait until the BUSY become inactive. In this duration, the processor extension is busy with its allotted job. Once the job is completed the processor extension drives the BUSY input high indicating 80286 to continue with the program execution. An active ERROR signal causes the 80286 to perform the processor extension interrupt while executing the WAIT and ESC instructions. The active ERROR signal indicates to 80286 that the processor extension has committed a mistake and hence it is reactivating the processor extension interrupt.

- **CAP:** A 0.047 µf, 12V capacitor must be connected between this input pin and ground to filter the output of the internal substrate bias generator. For correct operation of 80286 the capacitor must be charged to its operating voltage. Till this capacitor charges to its full capacity, the 80286 may be kept stuck to reset to avoid any spurious activity.

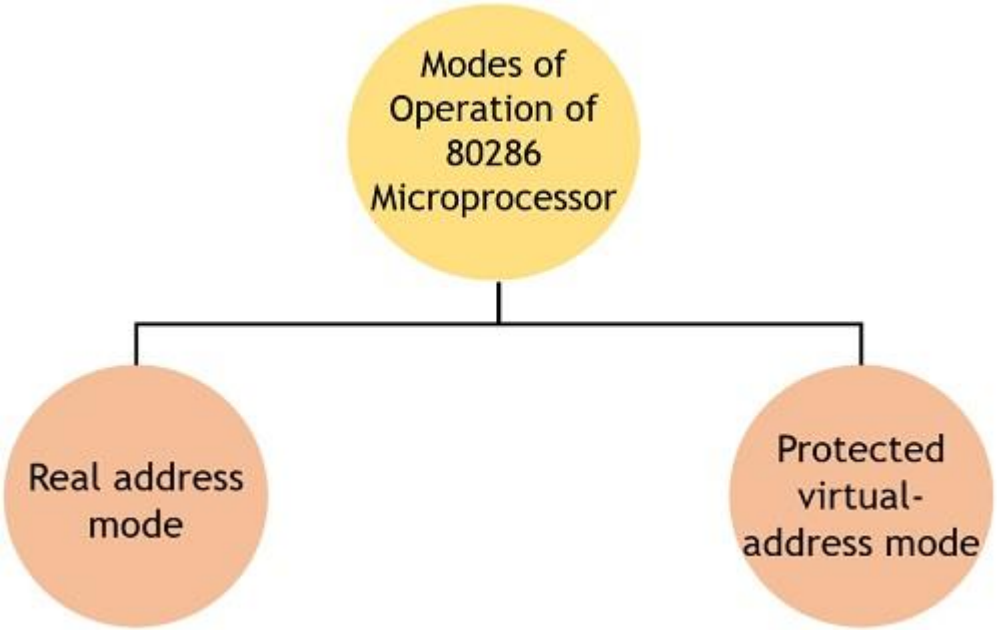
- **Vss:** This pin is a system ground pin of 80286.
- **Vcc:** This pin is used to apply +5V power supply voltage to the internal circuit of 80286. RESET The active-high RESET input clears the internal logic of 80286, and reinitializes it **RESET** The active-high reset input pulse width should be at least 16 clock cycles. The 80286 requires at least 38 clock cycles after the trailing edge of the RESET input signal, before it makes the first opcode fetch cycle.

Comparison of 80286 among some other microprocessor

Microprocessor	CPU Speed	Data bus	Address bus	Memory
8086	5 to 10 MHz	16	20	1M
80186	6 to 25 MHz	16	20	1M
80286	6 to 25 MHz	16	24	16M
80486	16 to 100 MHz	32	32	4G
Pentium 4	1.3 to 3.8 GHz	64	40	1T

Operating Modes

- operating modes of 80286 microprocessor
- 80286 operates in two modes:

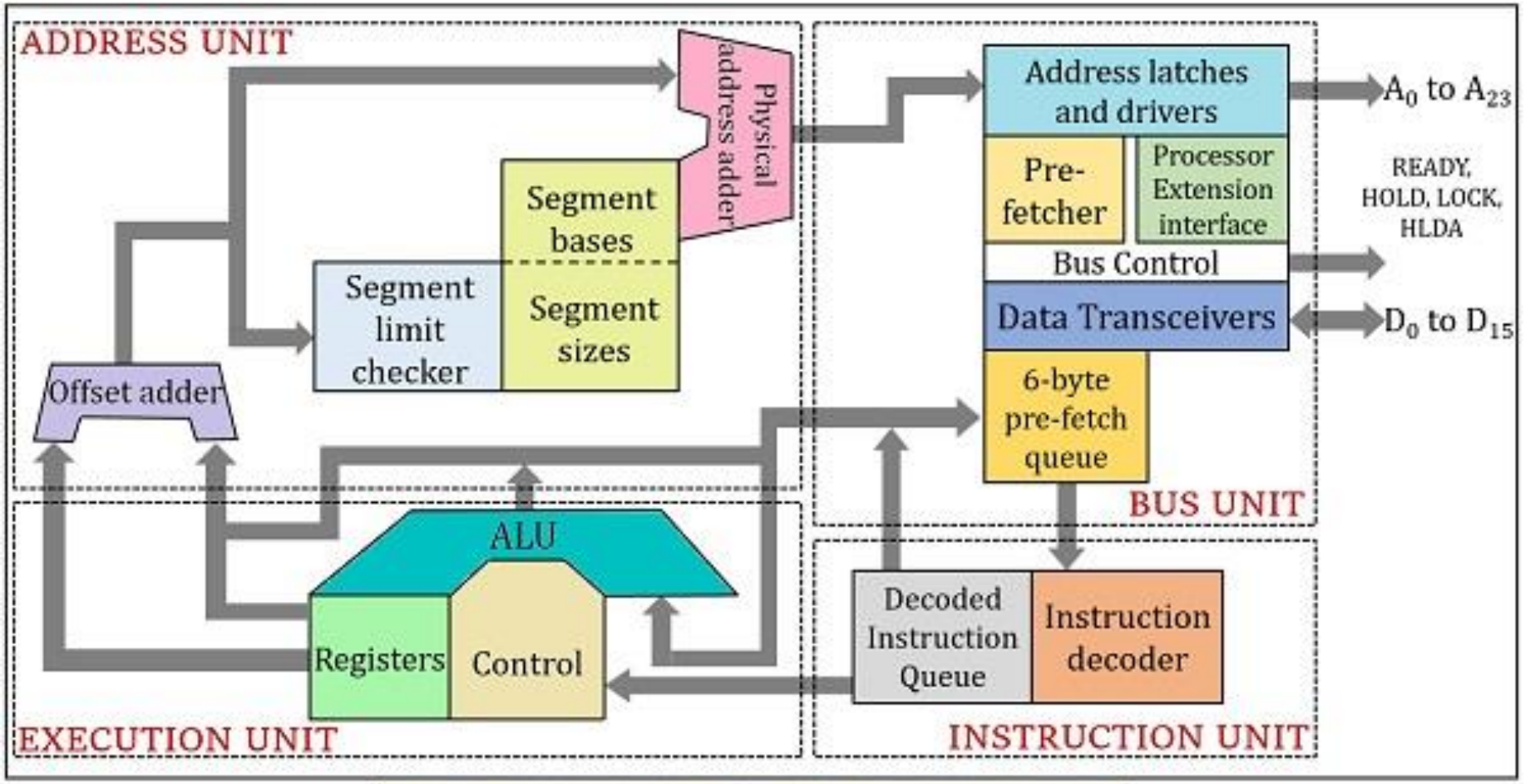


- **In real address mode**, this microprocessor acts as a version of 8086 which is quite faster. Also without any special modification, the instruction programmed for 8086 can be executed in 80286. It offers memory addressability of 1 MB of physical memory.
- The **protected virtual-address mode** of 80286 supports multitasking because multiple programs can be executed using virtual memory. This mode of 80286 offers memory addressability of 16 MB of physical memory along with 1 GB of virtual memory.
- As using virtual memory, space for other programs can be saved. Sometimes bulky programs also do exist that cannot be stored in physical memory, so virtual memory is utilized in order to execute large programs.
- This mode is used in 80286, so that in case of memory failure in real address mode, it can stay in protected manner.

What is virtual memory?

- Virtual memory is that part of hard disk which can be utilized for storing large instructions inside the system. This extra memory can be addressed by the computer other than the physical memory.
- When there exists an instruction that is to be loaded in the memory but whose size is greater than the provided physical memory. Then some part of hard disk is used in order to store that instruction, which is known as virtual memory.

Architecture of 80286 Microprocessor



Block Diagram of 80286 Microprocessor

- As we have already mentioned earlier that it is a 16-bit microprocessor thus holds a 16-bit data bus and 24-bit address bus. Also, unlike the 8086 microprocessor, it offers non-multiplexed address and data bus, which increases the operating speed of the system.
- 80286 is composed of nearly around 125K transistors and the pin configuration has a total of 68 pins.
- The CPU, central processing unit of 80286 microprocessor, consists of 4 functional block:
  - Address Unit
  - Bus Unit
  - Instruction Unit
  - Execution Unit

- Firstly, the physical address from where the data or instruction is to be fetched is calculated, by the **address unit**. Once the physical address is calculated then the calculated address is handed over to the **bus unit**. More specifically we can say, that the calculated address is loaded on the address bus of the bus unit.
- This address specifies the memory location from where the data or instruction is to be fetched. The fetching of data through the memory is done through the data bus. For faster execution of instruction, the BU fetches the instructions in advanced from the memory and stores them in the queue.
- This is done through the bus control module. As we have discussed that the prefetched instructions are stored in a **6-byte instruction queue**. This instruction queue then further sends the instruction to the **instruction unit**.
- The instruction unit on receiving the instructions now starts decoding the instruction. As instructions are stored in prefetched queue thus the decoder continuously decodes the fetched instructions and stores them into decoded instruction queue.

- Now after the instructions gets decoded then further these are needed to be executed. So, the instructions from decoded instruction queue are fed to the **execution unit**. The main component of EU is ALU i.e., arithmetic and logic unit that performs the arithmetic and logic operations over the operand according to the decoded instruction.
- Once the execution of the instruction is performed then the result of the operation i.e., the desired data is send to the register bank through the data bus.
- As we have already discussed that 80286 is just a modified version of 8086. The register set in 80286 is same as that of 8086 microprocessor.
- It holds 8 general purpose registers of **16 bit** each.
- It contains 4 segment register each of **16-bit**.
- Also has status and control register and instruction pointer.

Register Organization of 80286

The 80286 CPU contains almost the same set of registers as in 8086.

1. **Eight 16-bit general purpose registers.**
2. **Four 16-bit segment registers.**
3. **Status & Control register.**
4. **Instruction Pointer.**

The register set of 80286 is shown in Fig. 9.1.

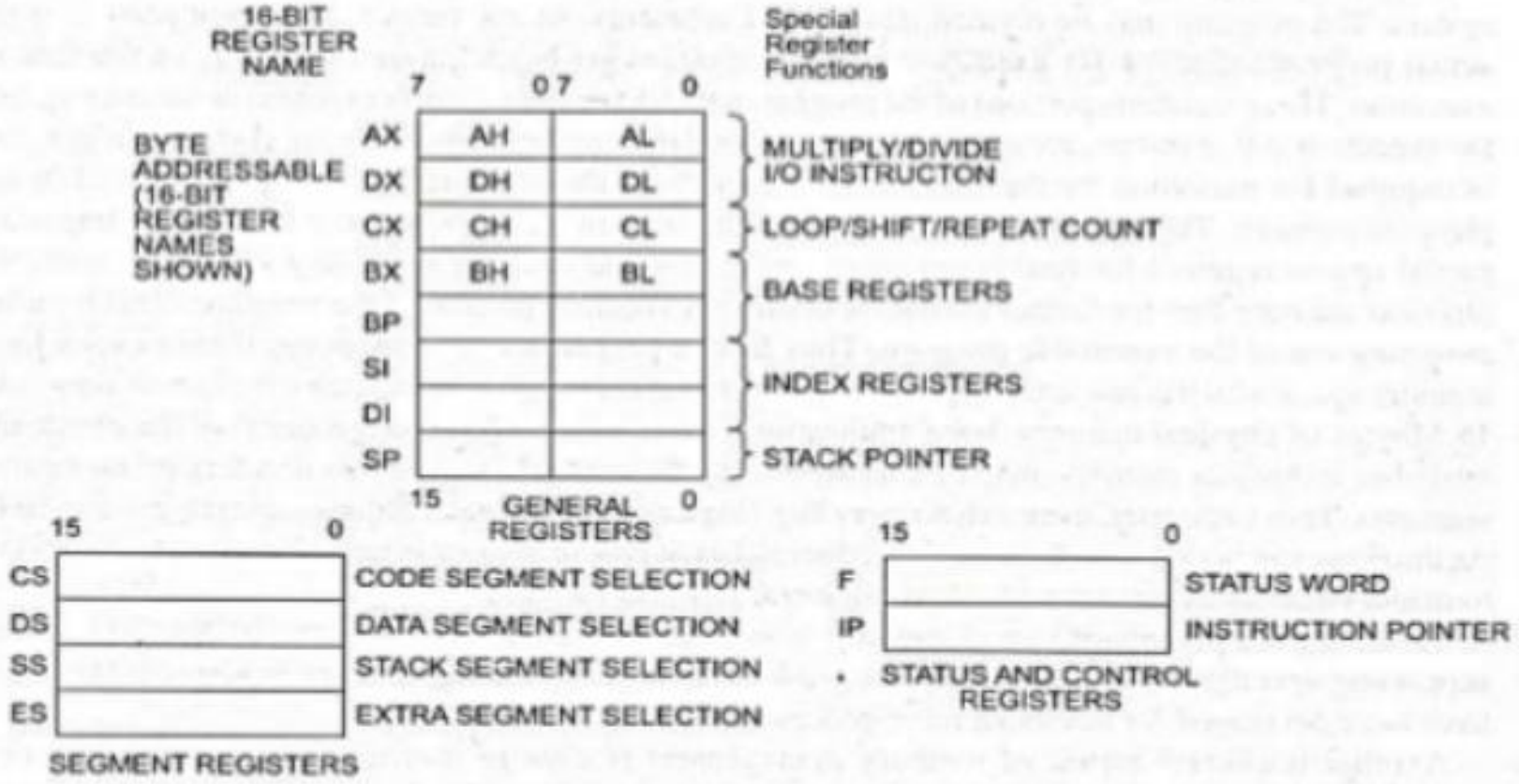


Fig. 9.1 *Register Set of 80286 (Intel Corp.)*

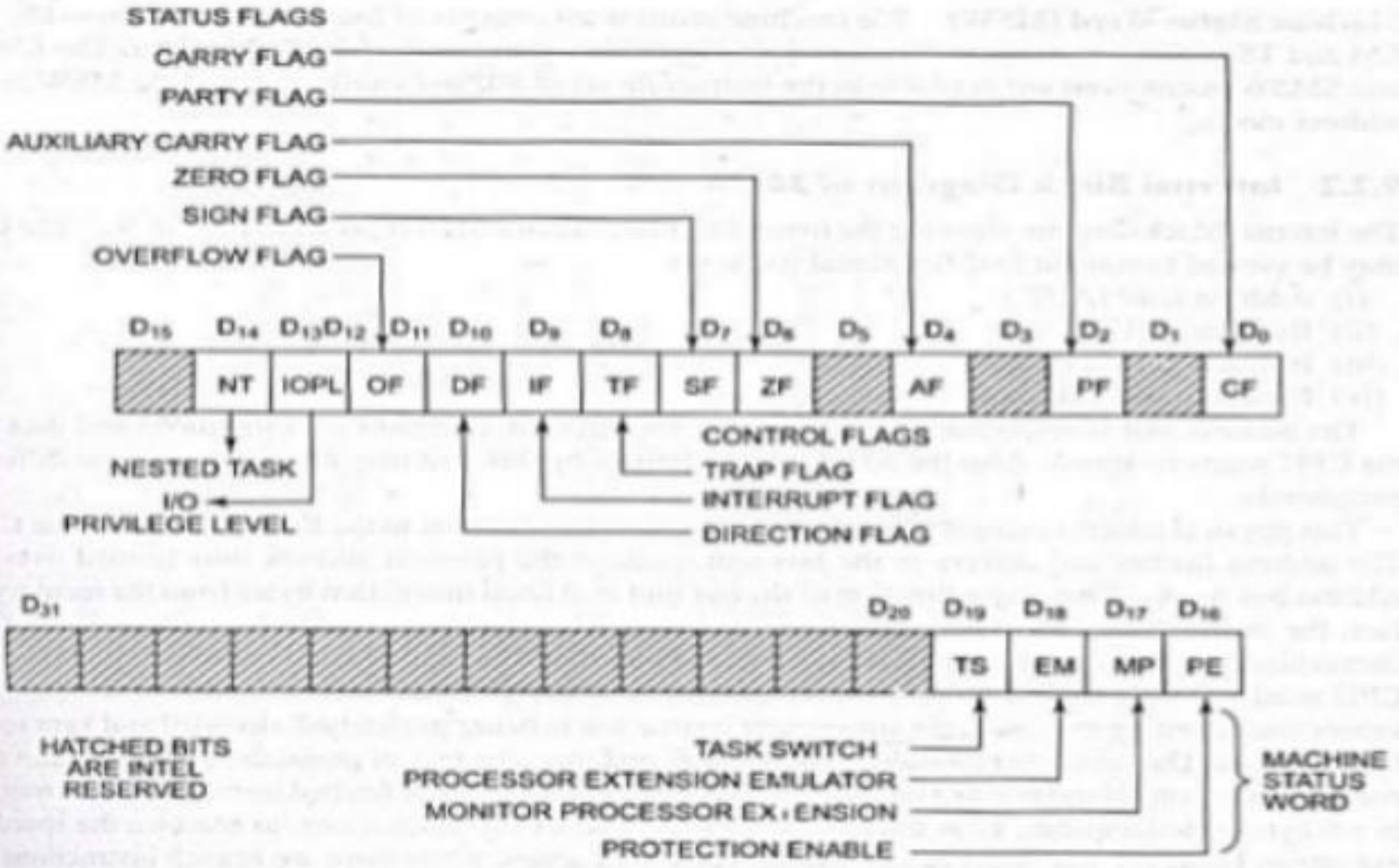


Fig. 9.2 *80286 Flag Register (Intel Corp.)*

Additional Instructions of Intel 80286

Sl no	Instruction	Purpose
1.	CLTS	Clear the task – switched bit
2.	LDGT	Load global descriptor table register
3.	SGDT	Store global descriptor table register
4.	LIDT	Load interrupt descriptor table register
5.	SIDT	Store interrupt descriptor table register
6.	LLDT	Load local descriptor table register
7.	SLDT	Store local descriptor table register
8.	LMSW	Load machine status register
9.	SMSW	Store machine status register

Instruction	Purpose
LAR	Load access rights
LSL	Load segment limit
SAR	Store access right
ARPL	Adjust requested privilege level
VERR	Verify a read access
VERW	Verify a write access

- **Thank u**